

VZ7A Block Diagram

PCB PTH Stackups

LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : SVCC
 LAYER 6 : IN3
 LAYER 7 : GND1
 LAYER 8 : IN4
 LAYER 9 : GND2
 LAYER 10 : BOT

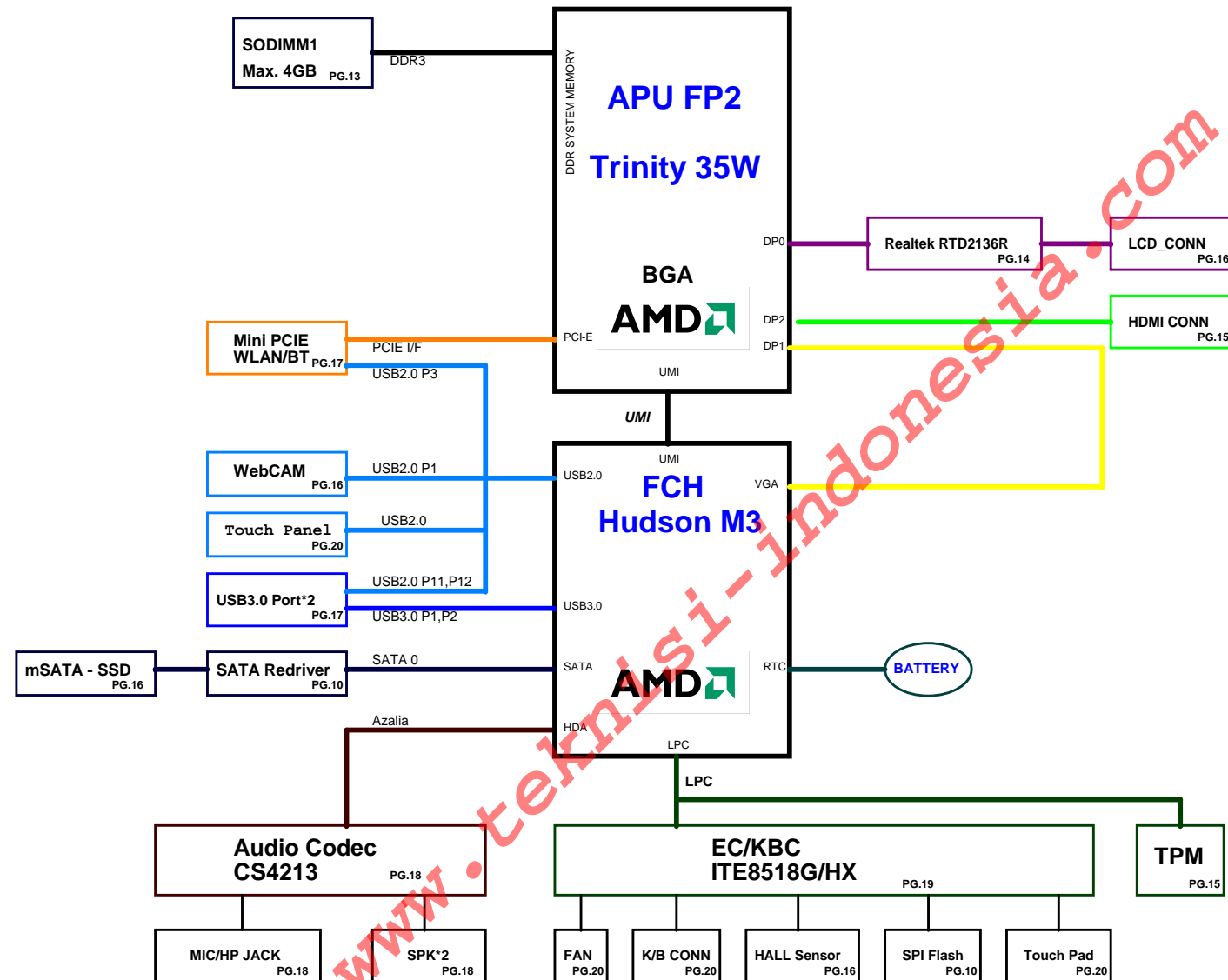


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Voltage Rails

Power	Voltage	S0	S3	S4/S5	S4/S5 (RTC wake)	S5+ (WLAN wake)	G3	Ctl Signal
VCCRTC	3V	ON	ON	ON	ON	ON	ON	
VIN	19.5V	ON	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	ON	OFF	Adaptor in
3V_S5_P	3.3V	ON	ON	ON	ON	ON	OFF	S5_ON1
3V_WLAN	3.3V	ON	ON	ON	ON	ON	OFF	WLAN_ON
12V_S5	12V	ON	ON	ON	ON	ON	OFF	Adaptor in
5V_S5	5V	ON	ON	ON	ON	ON	OFF	S5_ON1
3V_S5	3.3V	ON	ON	OFF	ON	OFF	OFF	S5_ON1
1.1V_S5	1.1V	ON	ON	OFF	ON	OFF	OFF	S5_ON2
5V_S3	5V	ON	ON	OFF	OFF	OFF	OFF	S3_ON
1.5V_S3	1.5V	ON	ON	OFF	OFF	OFF	OFF	S3_ON
5V_S0	5V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON_1
3V_S0	3V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON_1
2.5V_S0	2.5V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON_2
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON_2
DDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON_2
1.2V_S0	1.2V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON_2
1.1V_S0	1.1V	ON	OFF	OFF	OFF	OFF	OFF	S0_ON_2
NB_CORE	By VID	ON	OFF	OFF	OFF	OFF	OFF	VRON
CPU_CORE	By VID	ON	OFF	OFF	OFF	OFF	OFF	VRON

Power On Sequencing Timing Diagram

System Power Sequence W/O S5+

EC CONTROL SIGNAL

TRIG	MIN	MAX	Control signal	Time
T0	5s		3V_S5V to S5_ON	5s
T2			S5_ON1 to S5_ON2	500us
T3	10ms		S5_ON2 to S0_ODR1	10ms
T4			S0_ODR1 to S0_ODR2	200us
T5			S5_ON2 to VRON	15ms
T6			VRON to S0_ODR2	15ms

Power OFF sequence

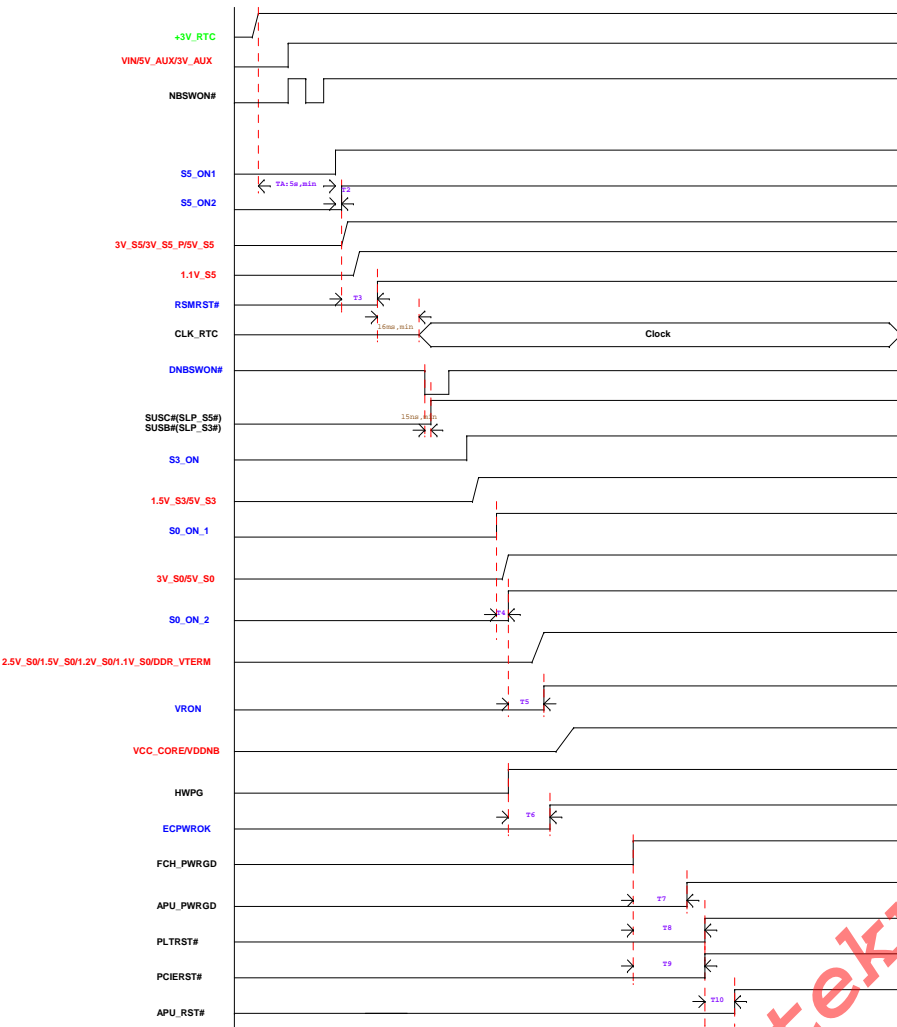
T8	NOTES		S5_ON2 to S0_ODR1	500us
T9	NOTES		S5_ON2 to S5_ON1	500us

System

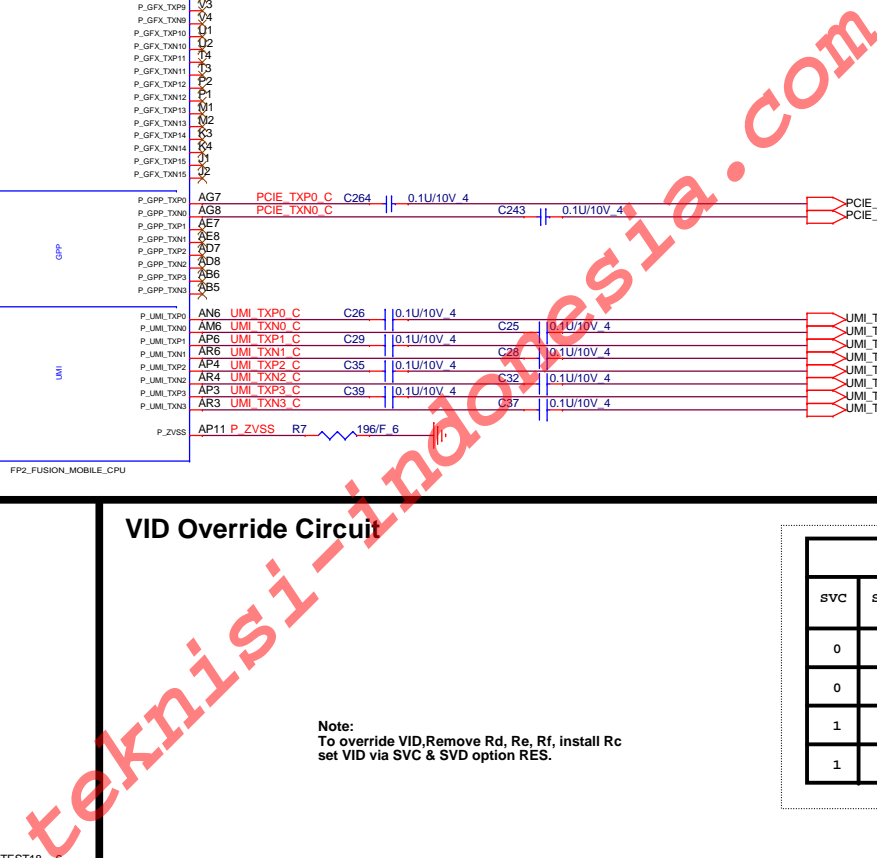
TRIG	MIN	MAX	Control signal	Time
T1	Time	50ms	PC1000 to S5_ON1	10ms
T2	10ms	15ms	PC1000 to S5_ON2	10ms
T3	10ms	15ms	PC1000 to S5_ON3	10ms
T4	1ms	2.5ms	PC1000 to S5_ON4	1.5ms

NOTE:

- 1.V_S5V to 1.1V_S5V (for system)
- 2.VDD3-VDD1 (for system)
- 3.VDD3-VDD1 (for up to 1000 converter)
- 4.VBAT to 3V_S5V to 1.1V_S5V must be greater than 5 seconds.
- 5.For power-down sequence, power rails on reference platform are either powered-down at the same time or in the reverse order of the power-up sequence.



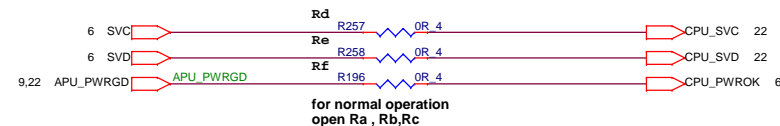
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VID Override Circuit



		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



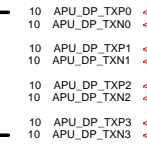
APU 3/4(Display/Misc)

06

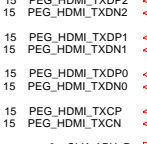
DP0 output to LVDS converter



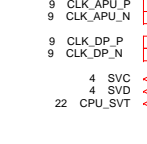
DP1 output to Hudson-M3 for VGA translator interface



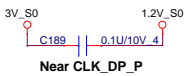
DP2 output to HDMI connector



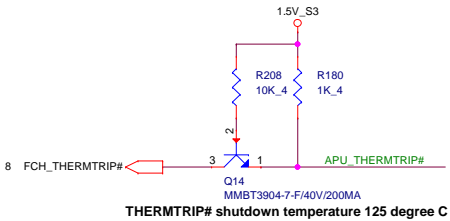
4.9 APU_RST#
4 CPU_PWROK



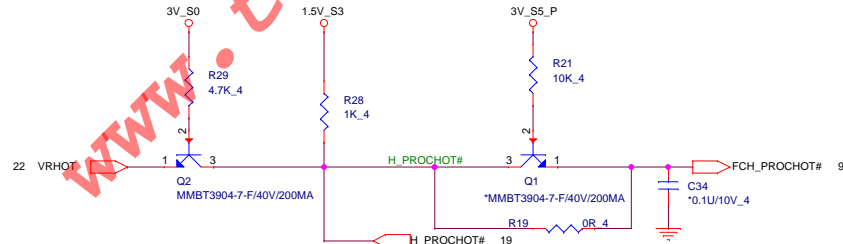
EMI



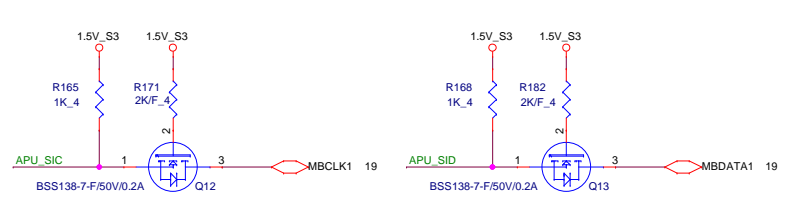
Thermal




Thermal Protect



SMBus

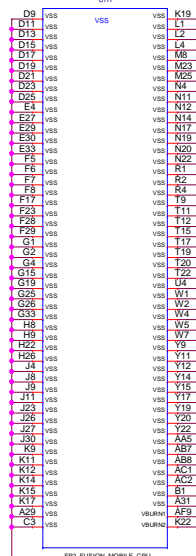
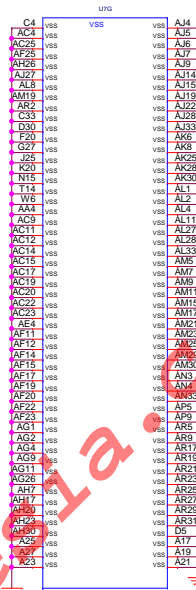
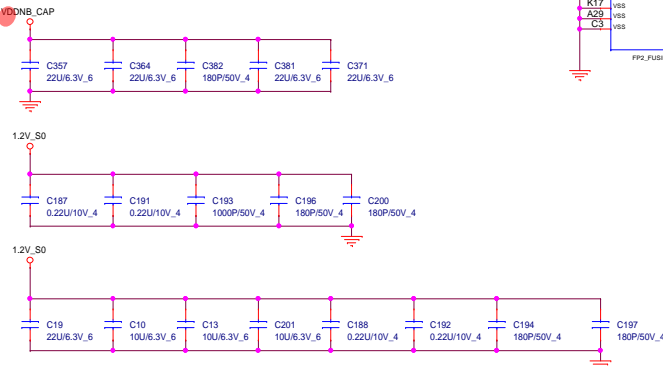




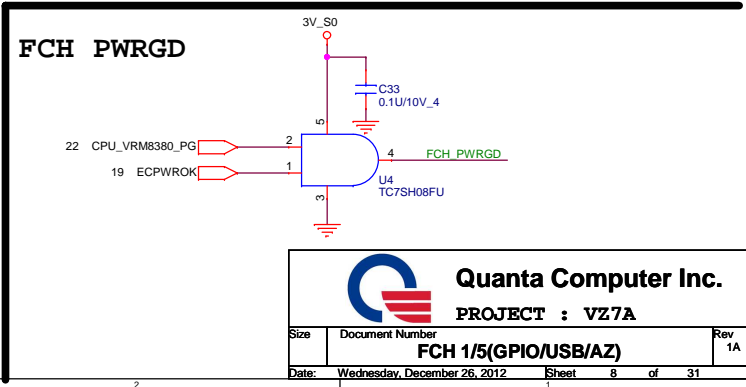
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PROJECT : VZ7A

Size	Document Number	Rev
	APU 3/4(Display/Misc)	1A
Date	Wednesday, December 26, 2012	Sheet 6 of 31

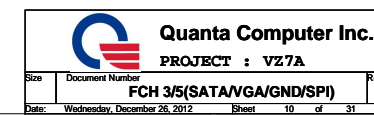
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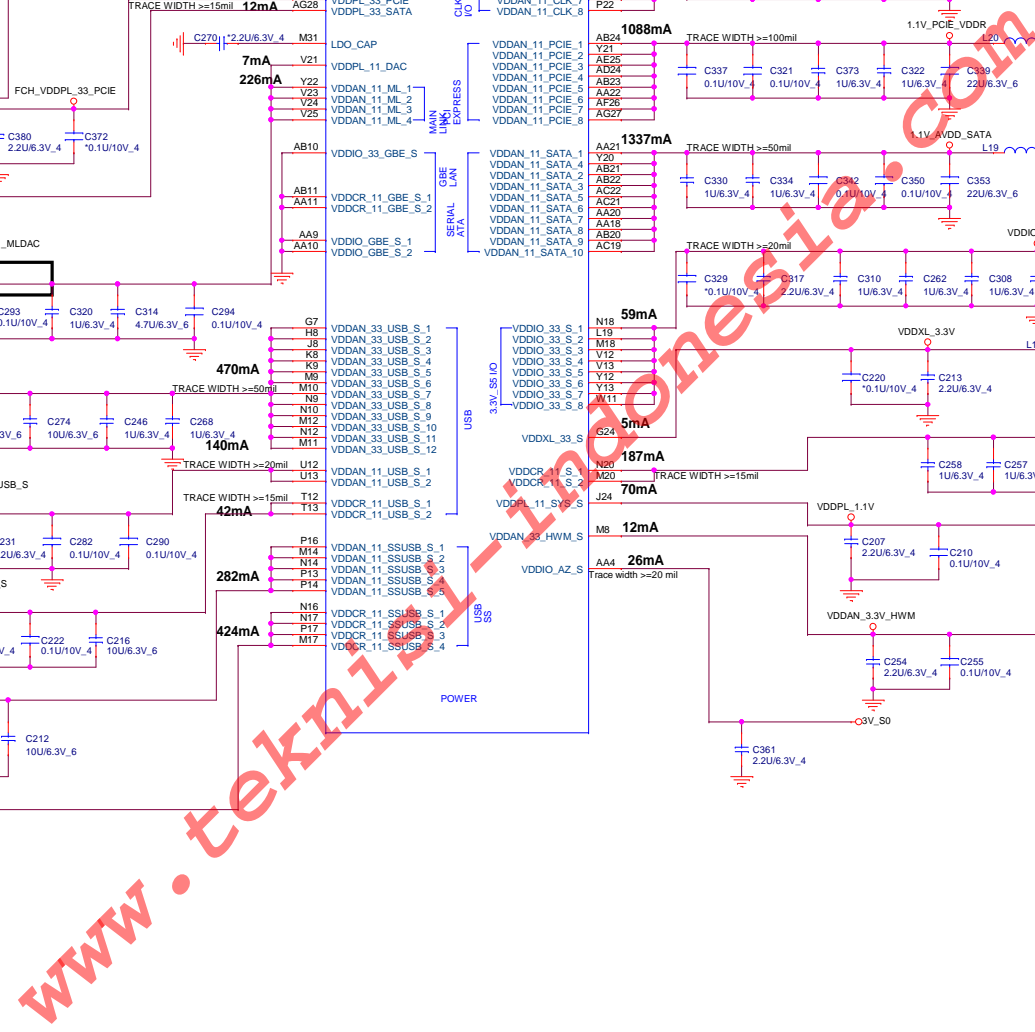
08





SPI ROM

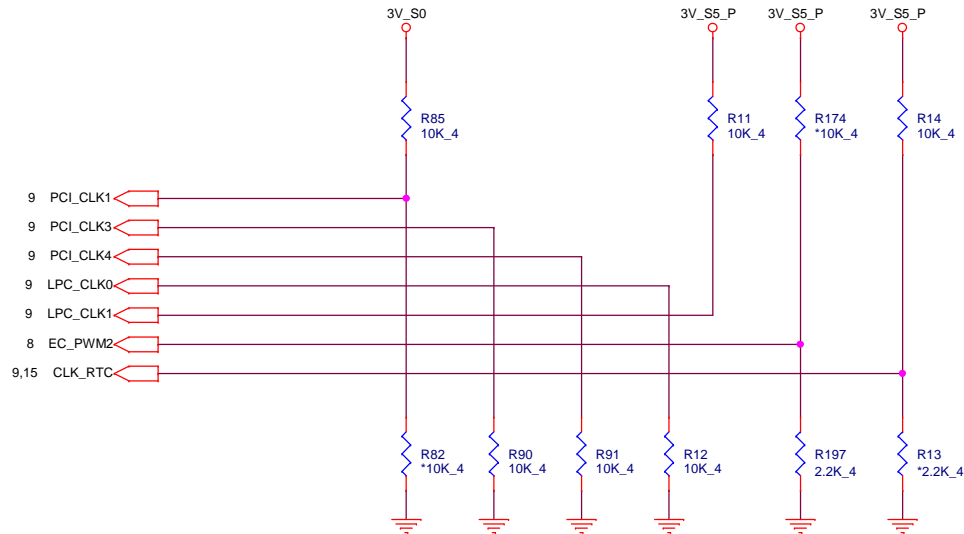




STRAPS PINS



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

Strap Pin	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
HIGH	ALLOW PCIE Gen2	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED	LPC ROM	S5 PLUS MODE DISABLED
LOW	FORCE PCIE Gen1	IGNORE DEBUG STRAP	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE

DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



remove reserve pull low resistor reserve test point only.

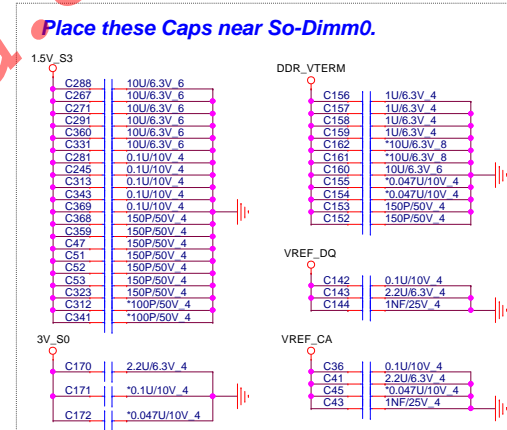
Strap Pin	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



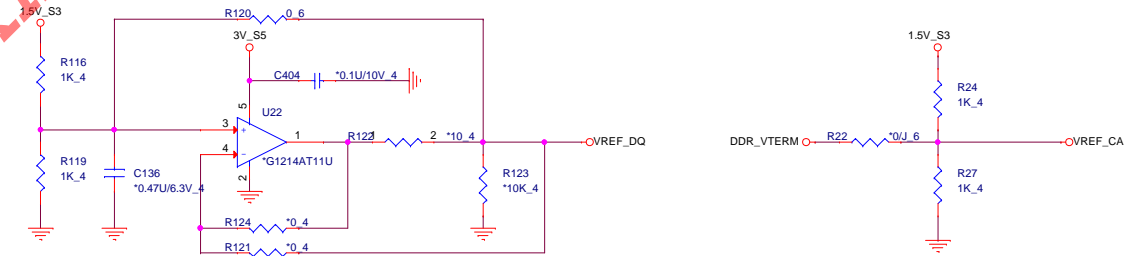
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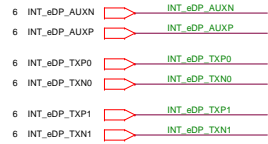
PROJECT : VZ7A

Size	Document Number	Rev
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Date:	Wednesday, December 26, 2012	Sheet 12 of 31



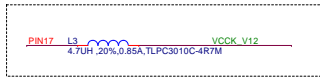
Reserved for AMD suggest



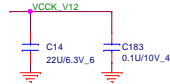


	2.2-uH(L3)	0 Ohm(R15)
SWR	Connect	NC
LDO	NC	Connect

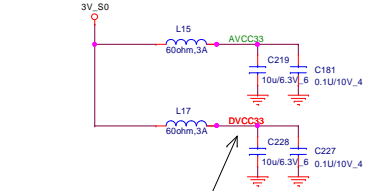
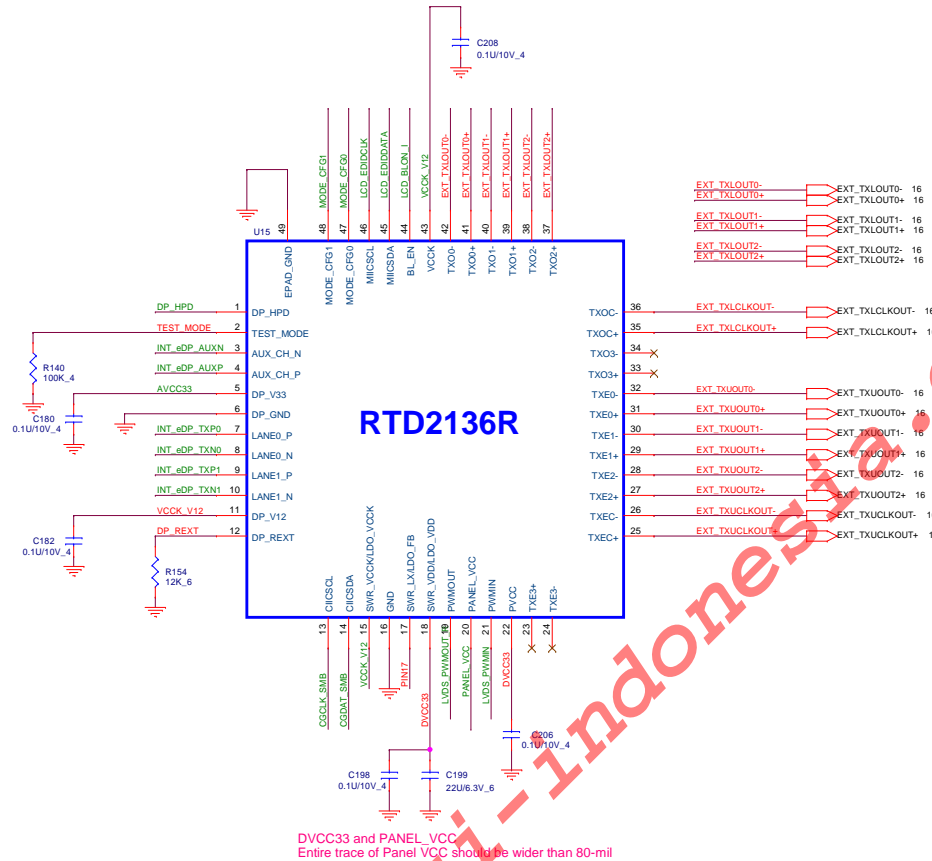
SWR MODE



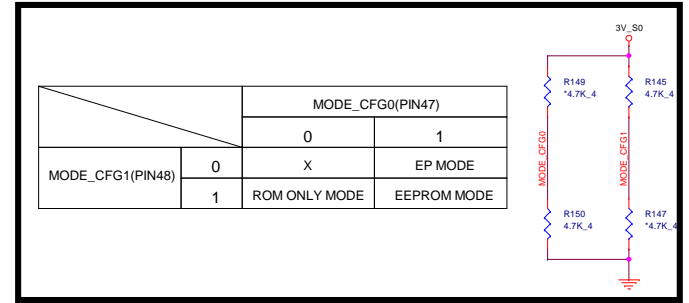
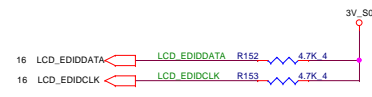
LDO MODE



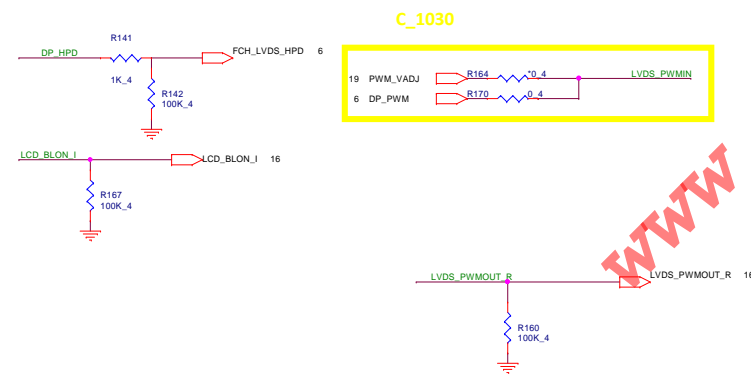
1. C41 10-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN17



Note:
1. Entire trace of Panel VCC should be wider than 80-mil



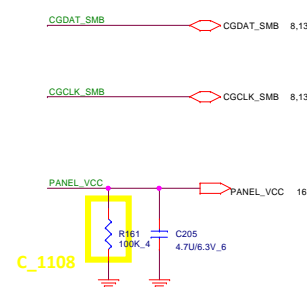
HPD/ Back Light/ BL PWM



Reserve EEPROM Address=0xA8

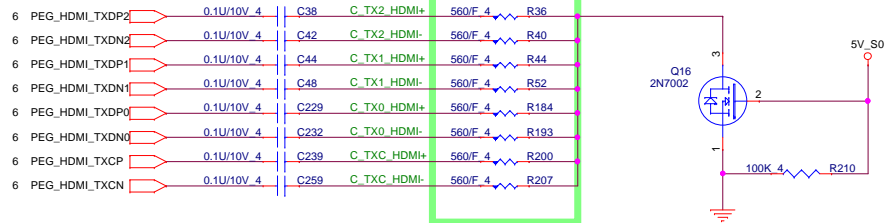


SMBUS & Panel VCC



HDMI

D_1210

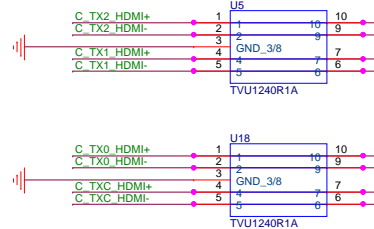


C_1080

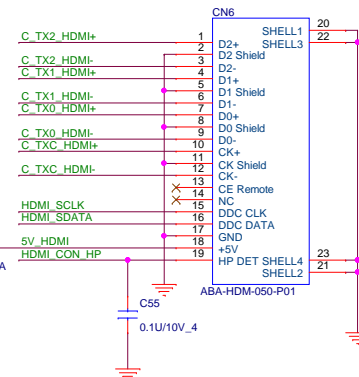
EMI D_1210

C_TX2_HDMI+	R35	180F_4	C_TX2_HDMI-
C_TX1_HDMI+	R43	180F_4	C_TX1_HDMI-
C_TX0_HDMI+	R183	180F_4	C_TX0_HDMI-
C_TXC_HDMI+	R199	180F_4	C_TXC_HDMI-

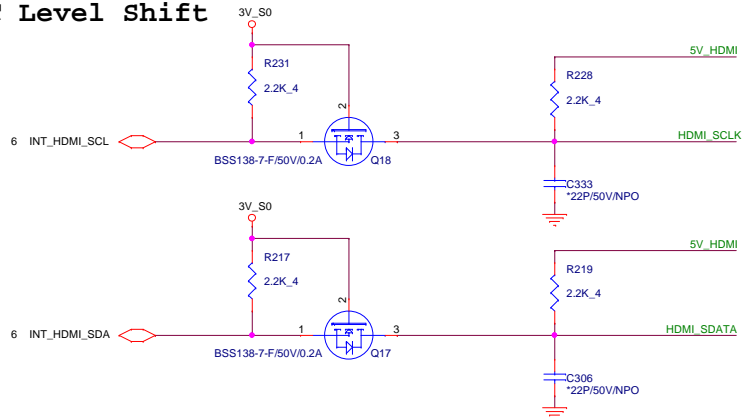
ESD



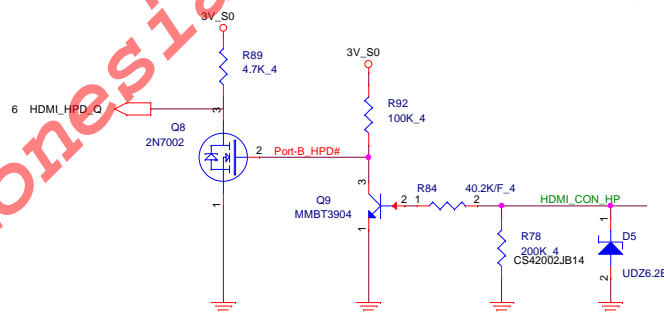
15



DDC Level Shift



HPD

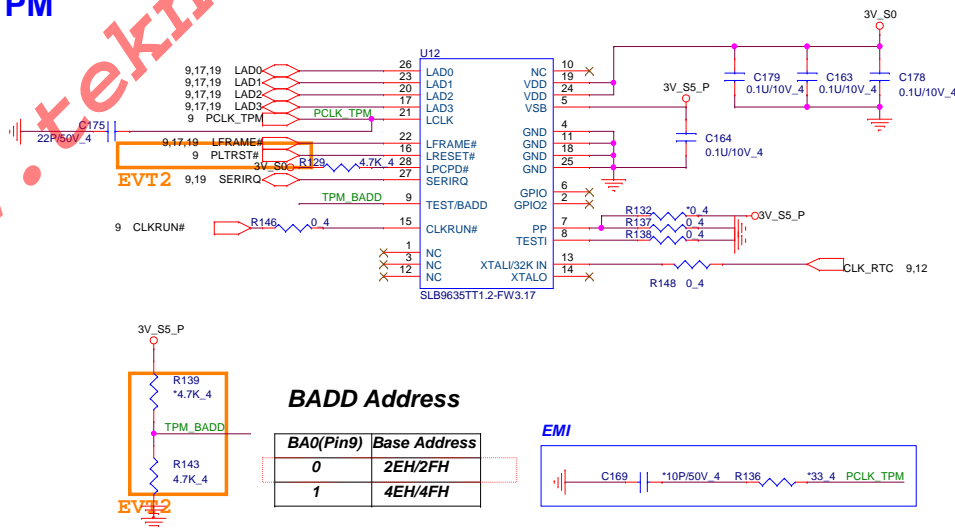


CRT

C_1107



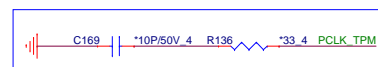
TPM



BADD Address

BA0(Pin9)	Base Address
0	2EH/2FH
1	4EH/4FH

EMI

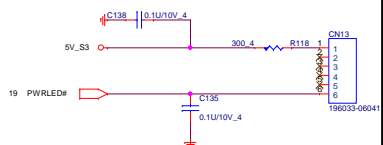


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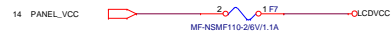
LED

0.2A(20mils)

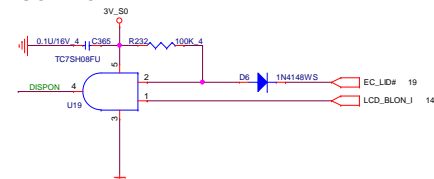


LCD POWER SWITCH

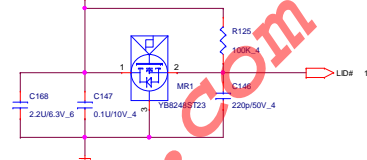
C_1025



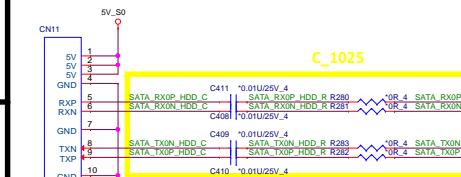
PANEL BACKLIGHT CONTROL



HALL SENSOR&BACK LIGHT SWITCH

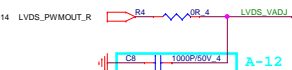
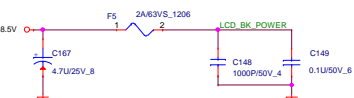


SATA (SATA over FFC)

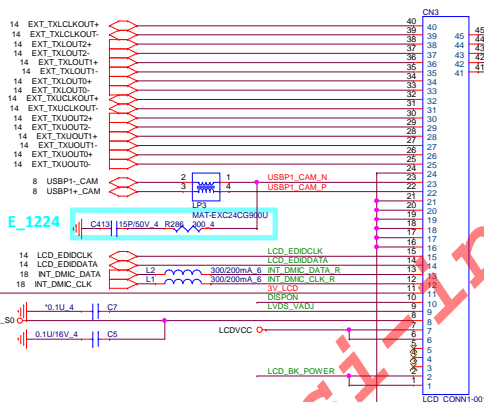
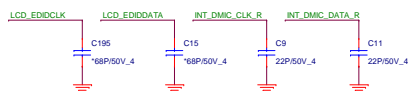


	SSS	2.5" SED
Der-Cap	C393/C395/C398/C400	C408/C409/C410/C411
bypass R		R280/R281/R282/R283

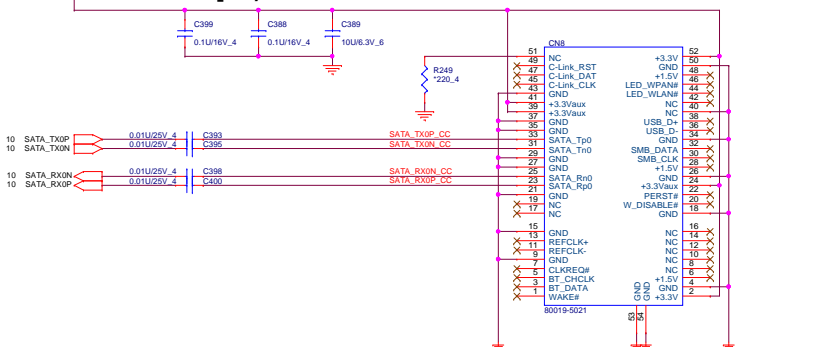
LCD Panel Module



For EMI close to connector



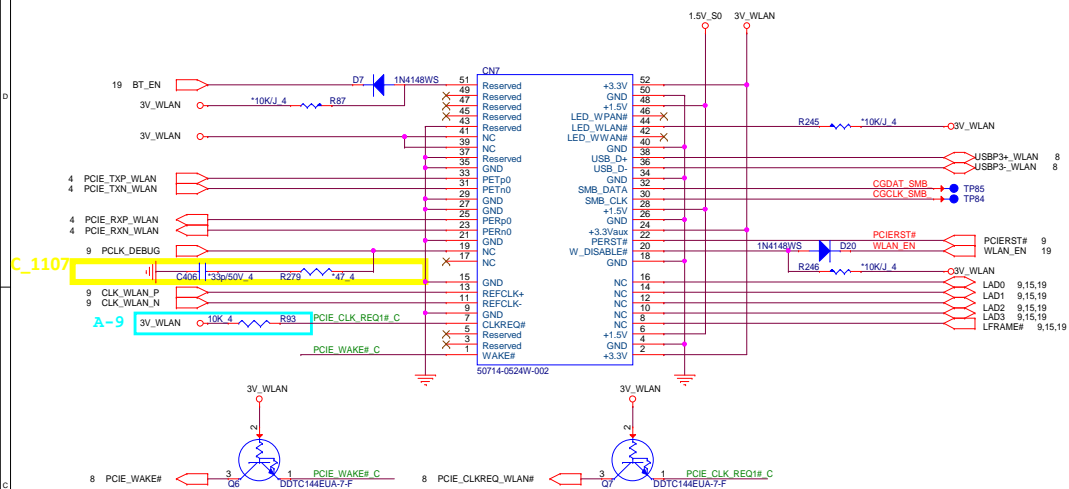
mSATA (SATA over mini PCIe)

128GB Write peak 4W, current 1.33A
Via need 2pcs, trace need 60mil

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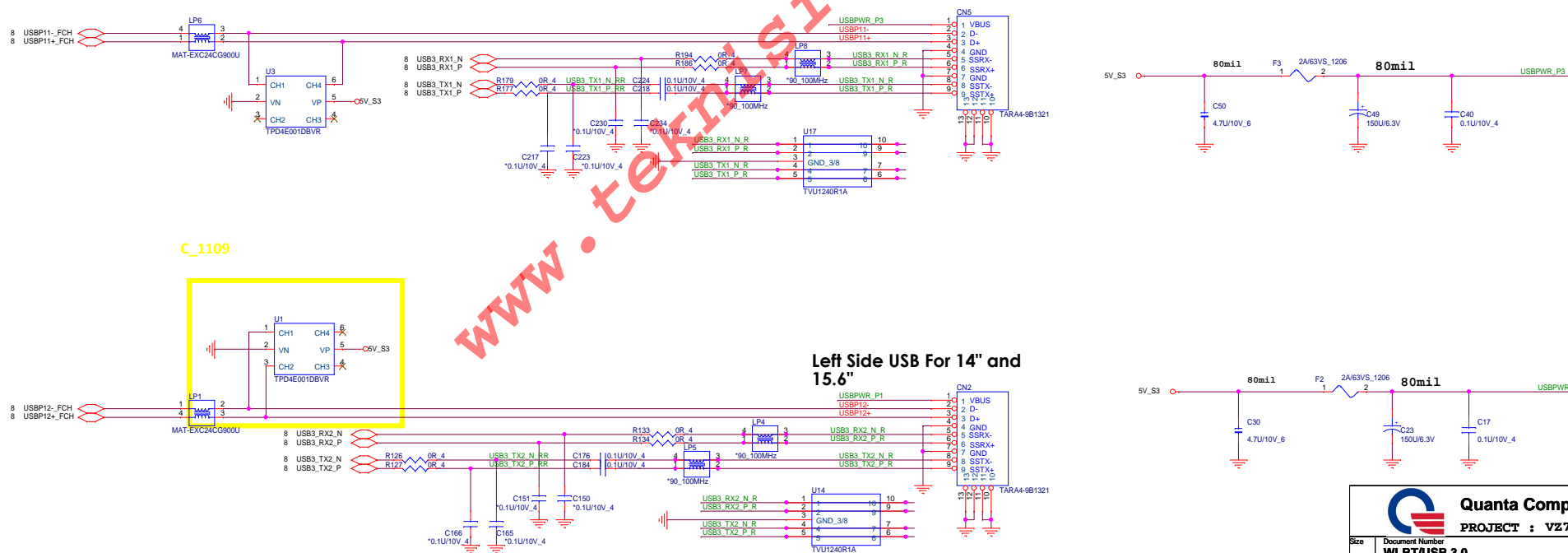
Size	Document Number	Rev
1A	LVDS/CCD/LED/mSATA	1A

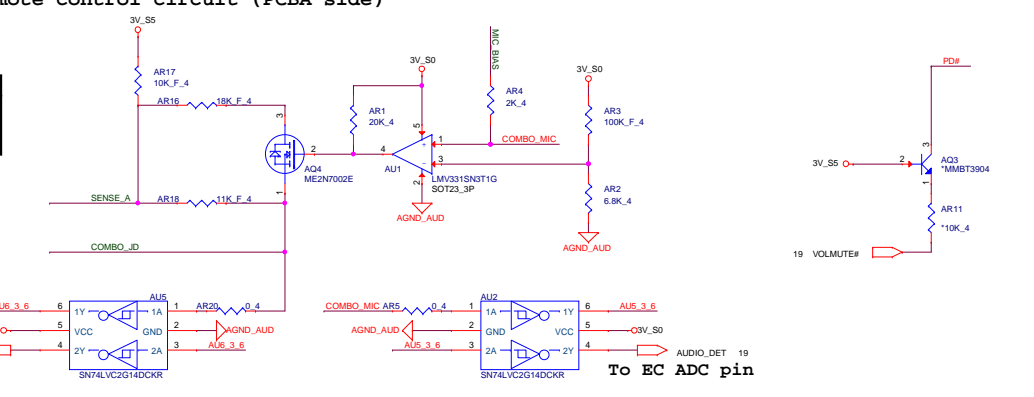
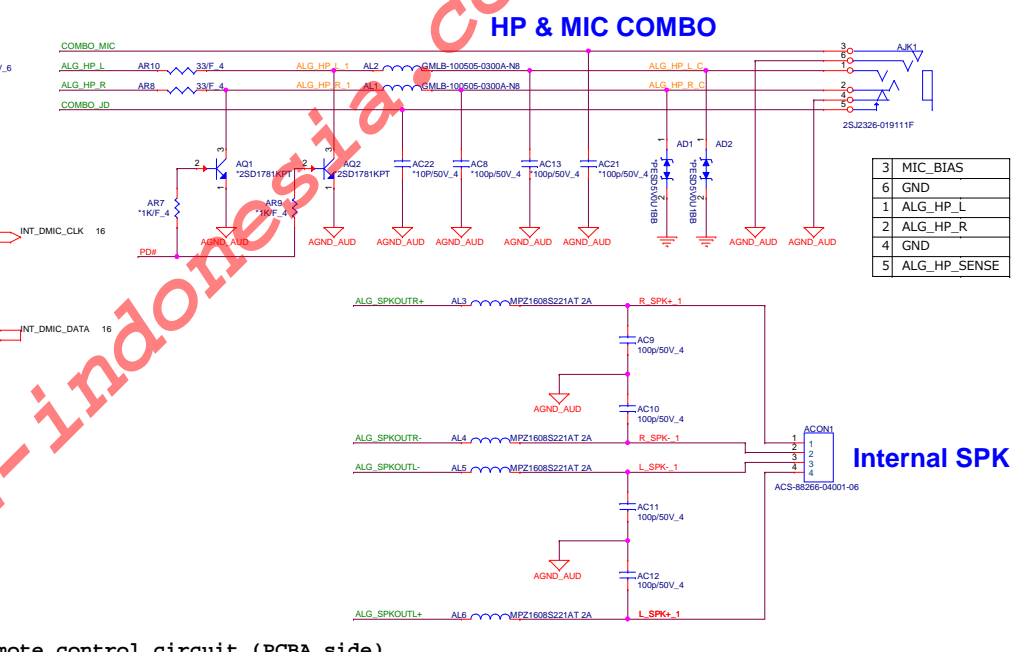
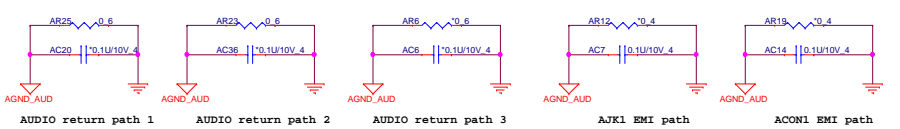
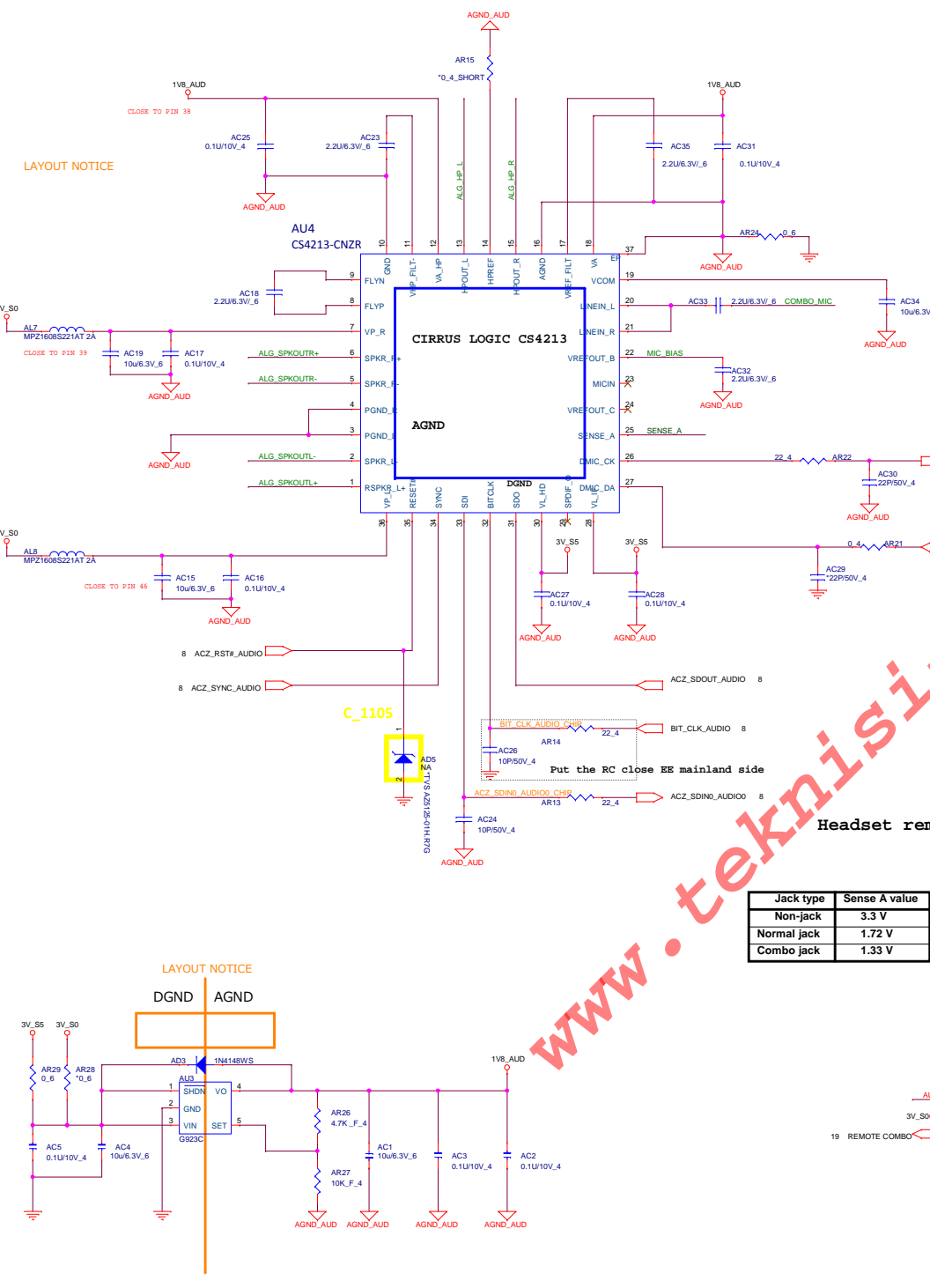
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USB 3.0

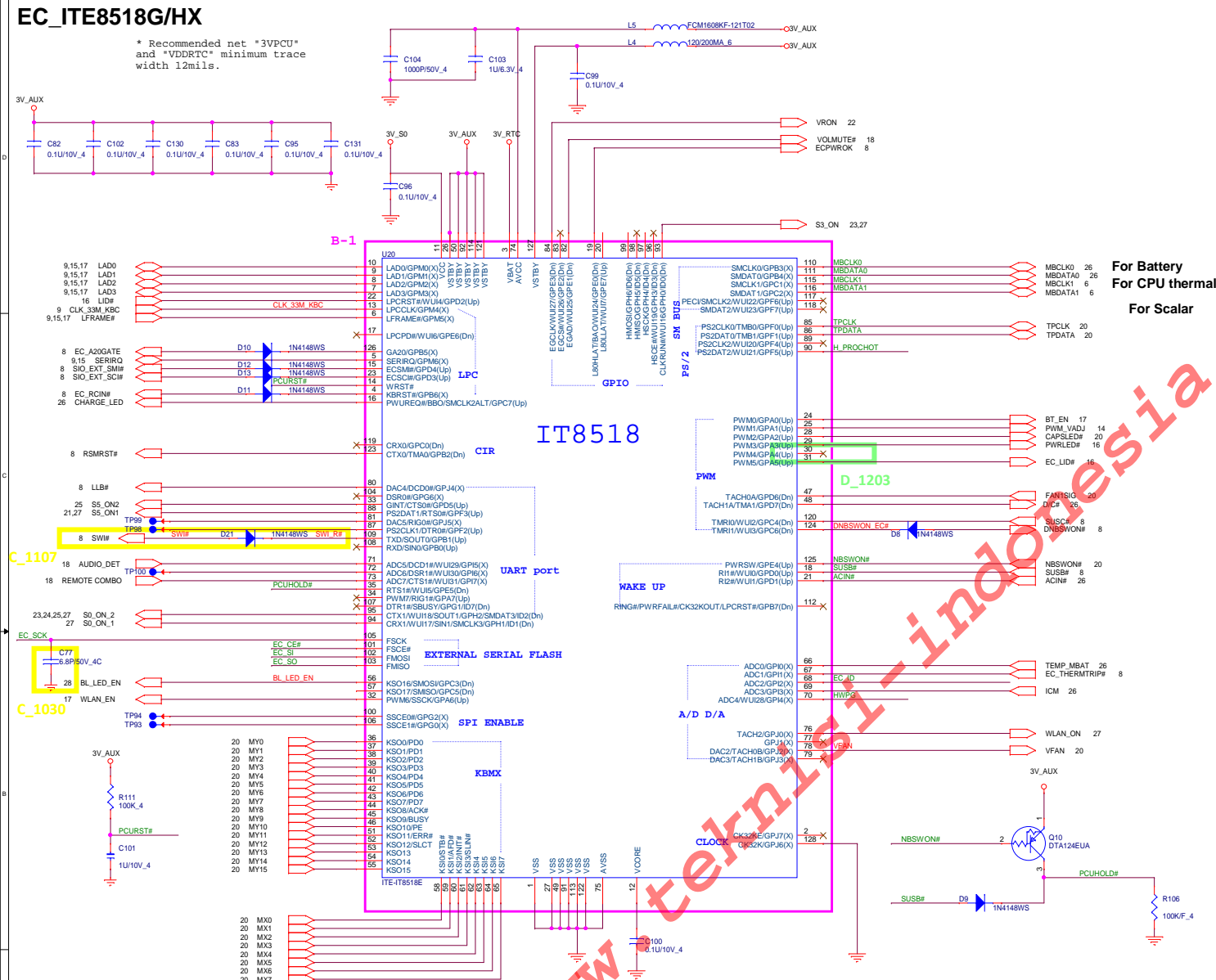
Right Side for 15.6 only



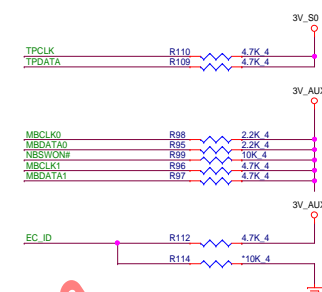


EC_ITE8518G/HX

* Recommended net "3VPCU"
and "VDDRTC" minimum trace
width 12mils.

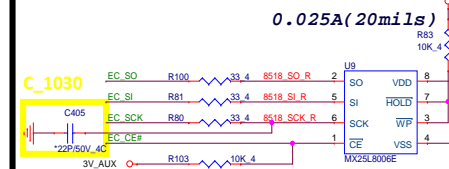


For Battery
For CPU thermal
For Scalar

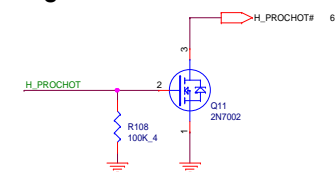


VZ7A	R113	Hi
VZ8A	R114	Lo

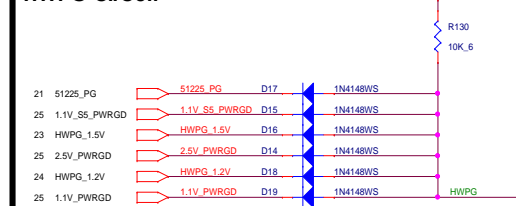
EC ROM 1MB



For throttling

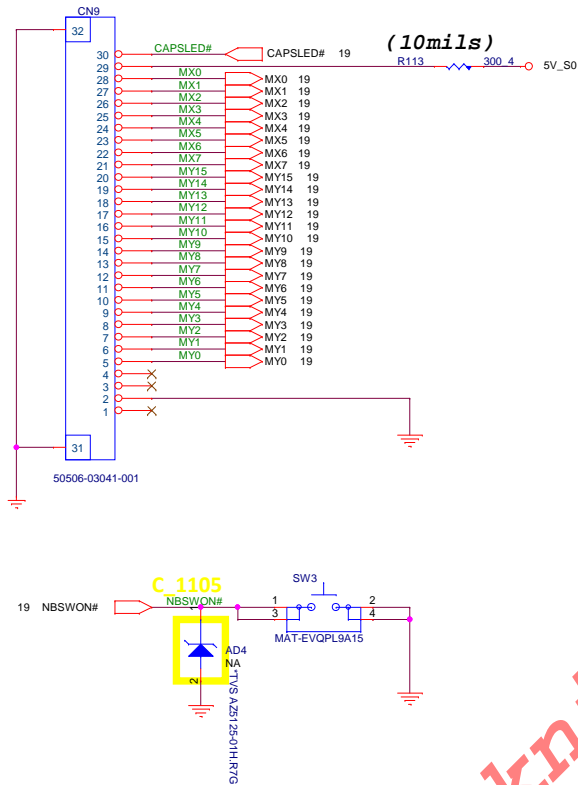


HWPG circuit

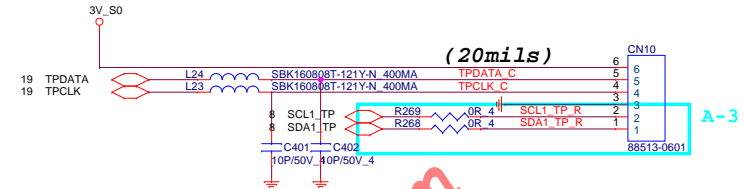


Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

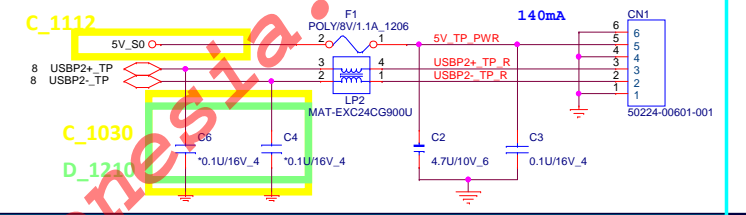
INT KeyBoard



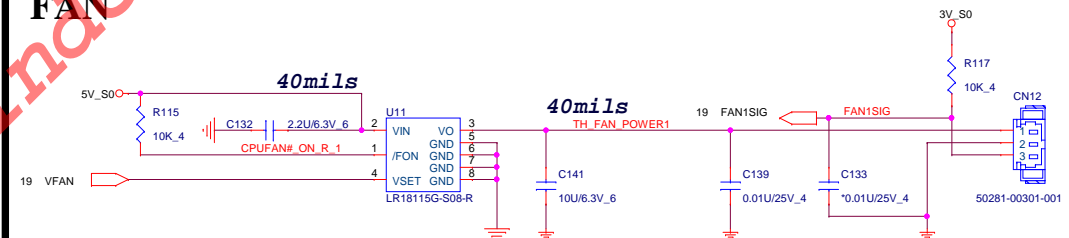
TP board



Touch Module



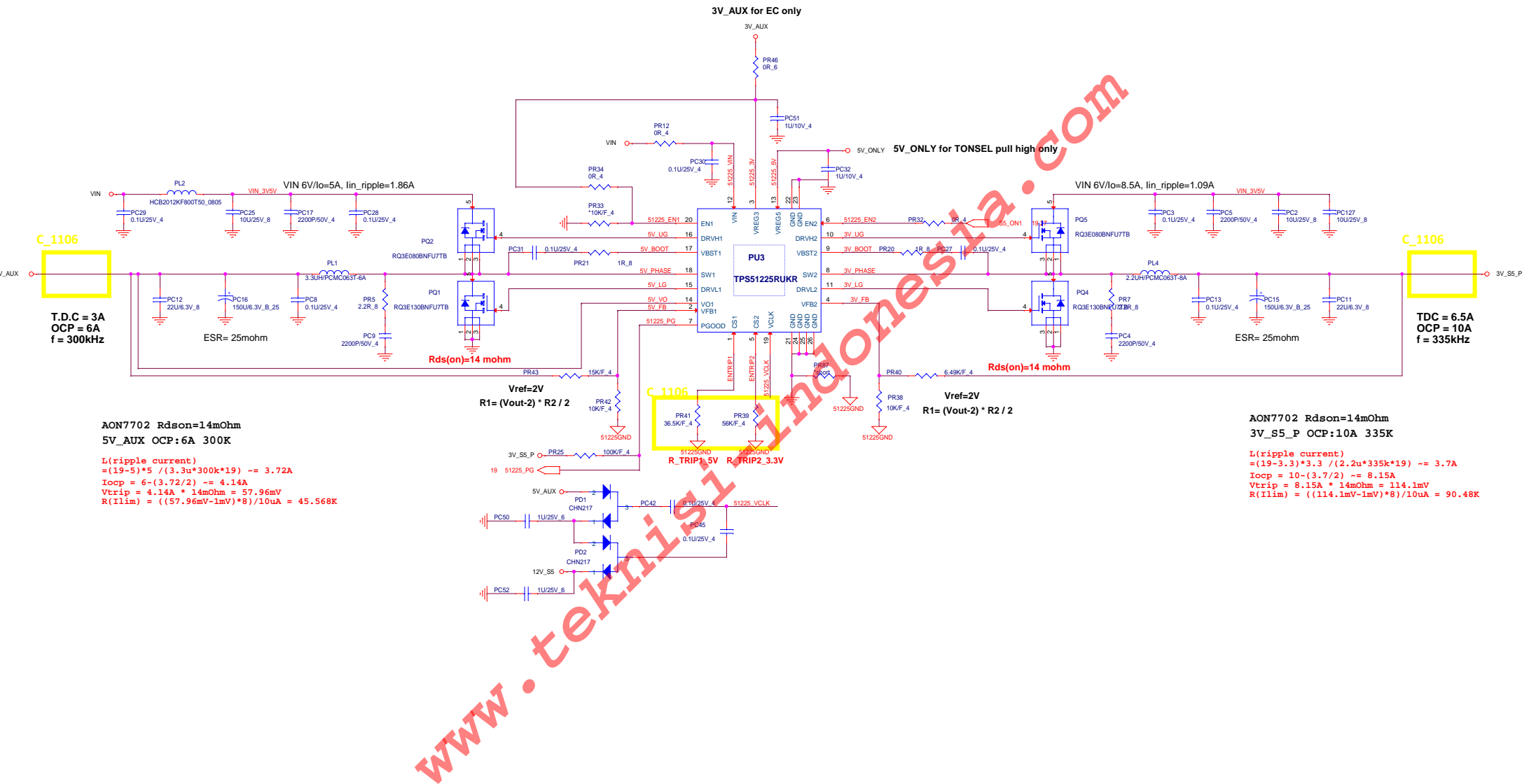
FAN



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Size	Document Number	Rev
TP/KB/FAN/Touch Module		1A

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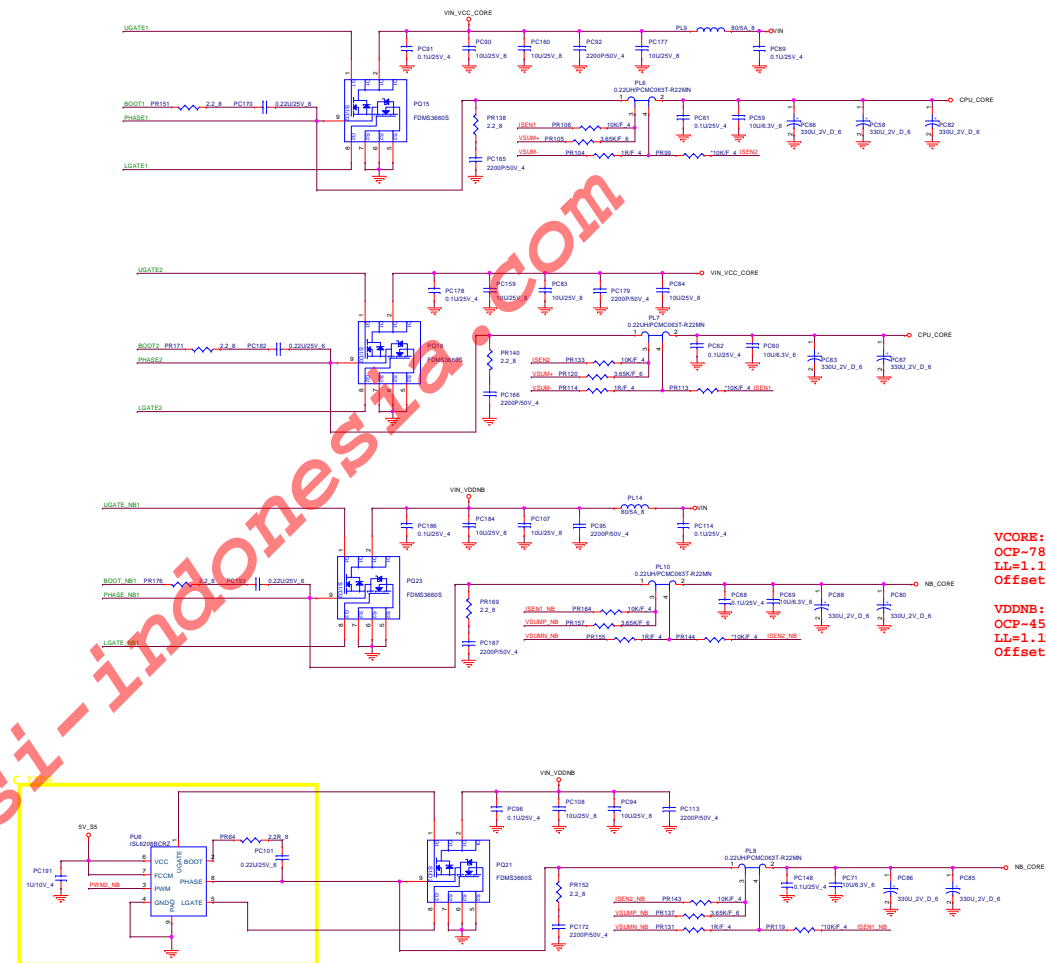
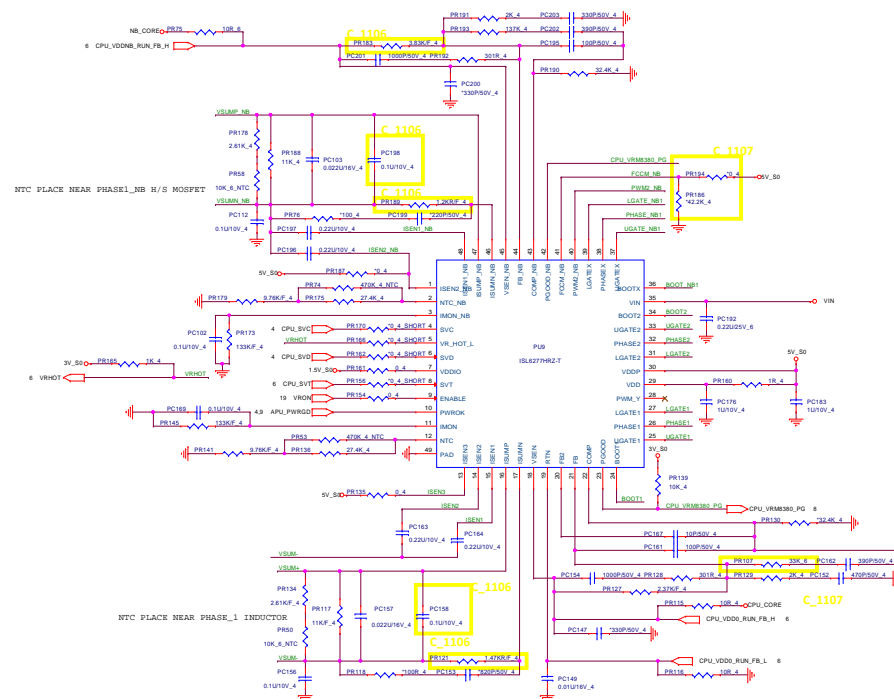
$I_{ripple} = (V_{in} - V_{out}) * V_{out} / (V_{in} * L * f)$

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V	14m_Max	6	3.72	300	3.3uH	45.3K
3.3V	14m_Max	10	3.7	335	2.2uH	90.9K

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON



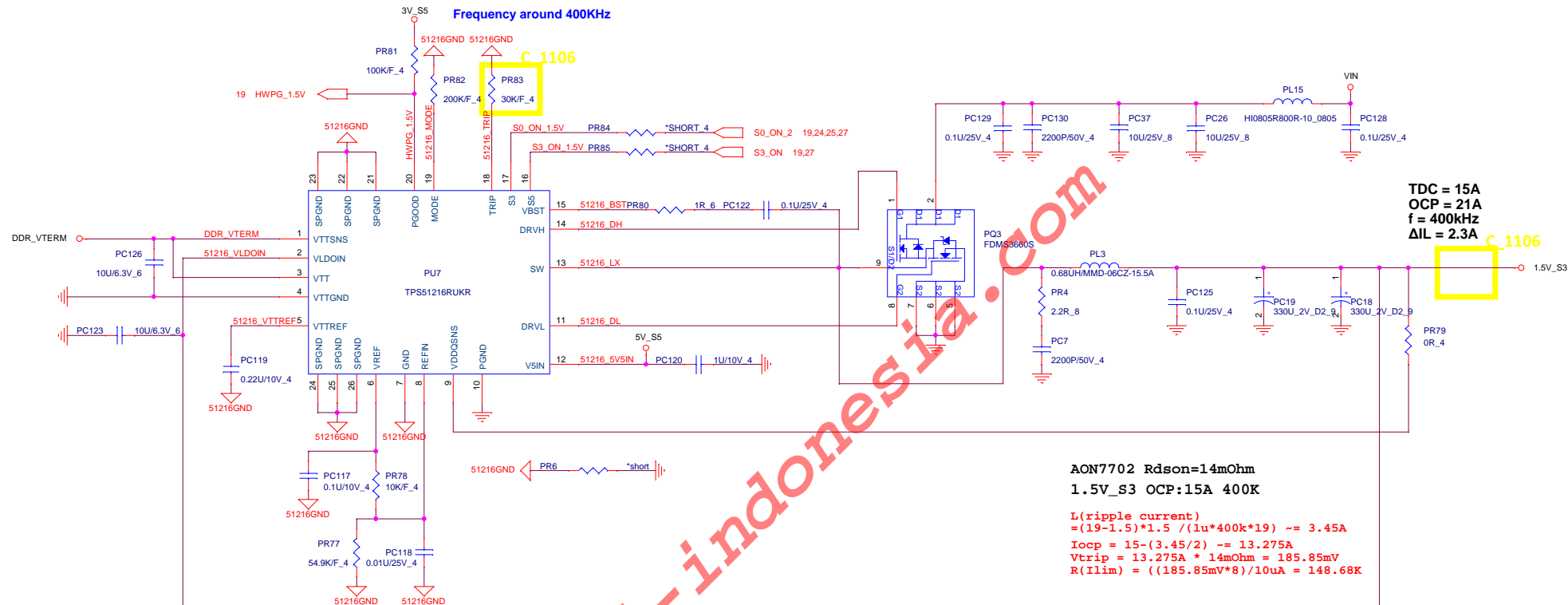
Vcore:
OCP~78A
LL=1.1mOhm
Offset=0mV

VDDNB:
OCP~45A
LL=1.1mOhm
Offset=0mV

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Footprint
0.22uH 20%	API	CV+22NM0M204	30	50	2.8m Max.	7X7X3	choke-pcnc063t-r82mm-4p

DDR3 1.5V_S3 (TPS51216RUKR)



$$I_{ripple} = (V_{in} - V_{out}) * V_{out} / (V_{in} * L * f)$$

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.5V	14m_Max	15	3.45	400	1uH	11.5K

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max
FDMC7692S	DFN 3*3	12.5A/18A	12m
AON7702	DFN 3*3	13.5A/20A	14m

21,22,26,27 VIN
22,24,25,27,29 5V_S5
4,5,6,7,13,24,25,29 1.5V_S3
13 DDR_VTERM



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Size

Document Number

DDR3 1.5V_S3 (TPS51216RUKR)

Rev

1A

Date

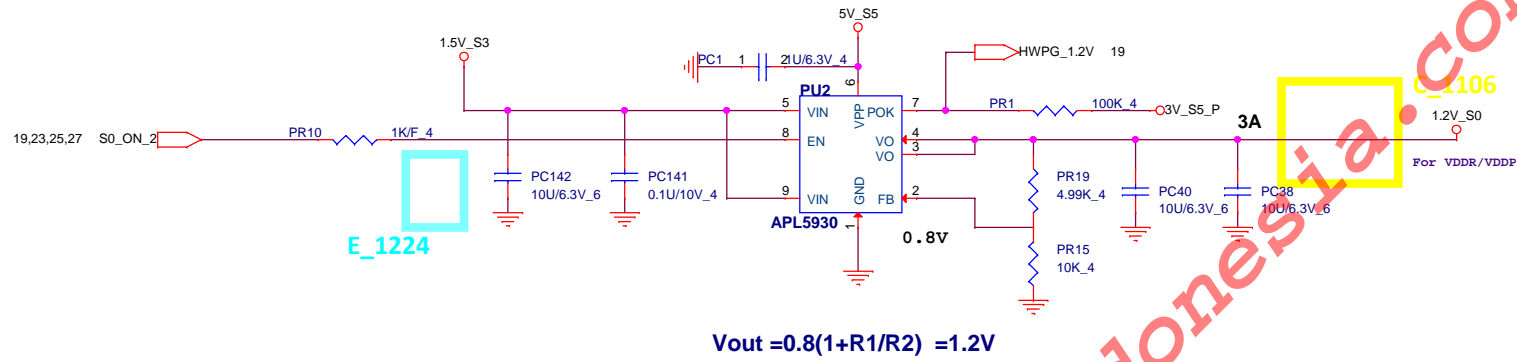
Wednesday, December 26, 2012

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of

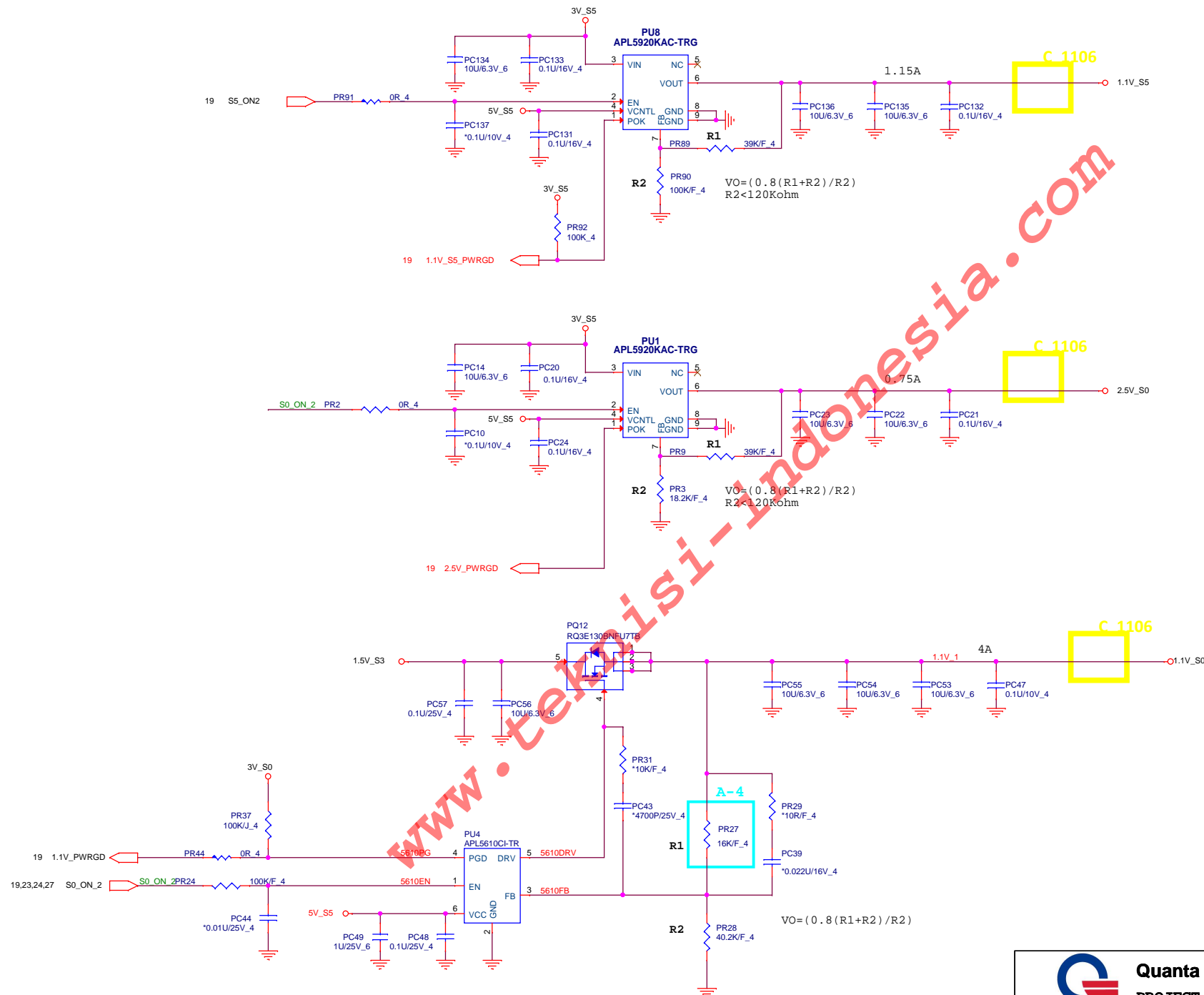
31



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Size	Document Number	Rev
	1.2V(RT8202AGQW)	1A
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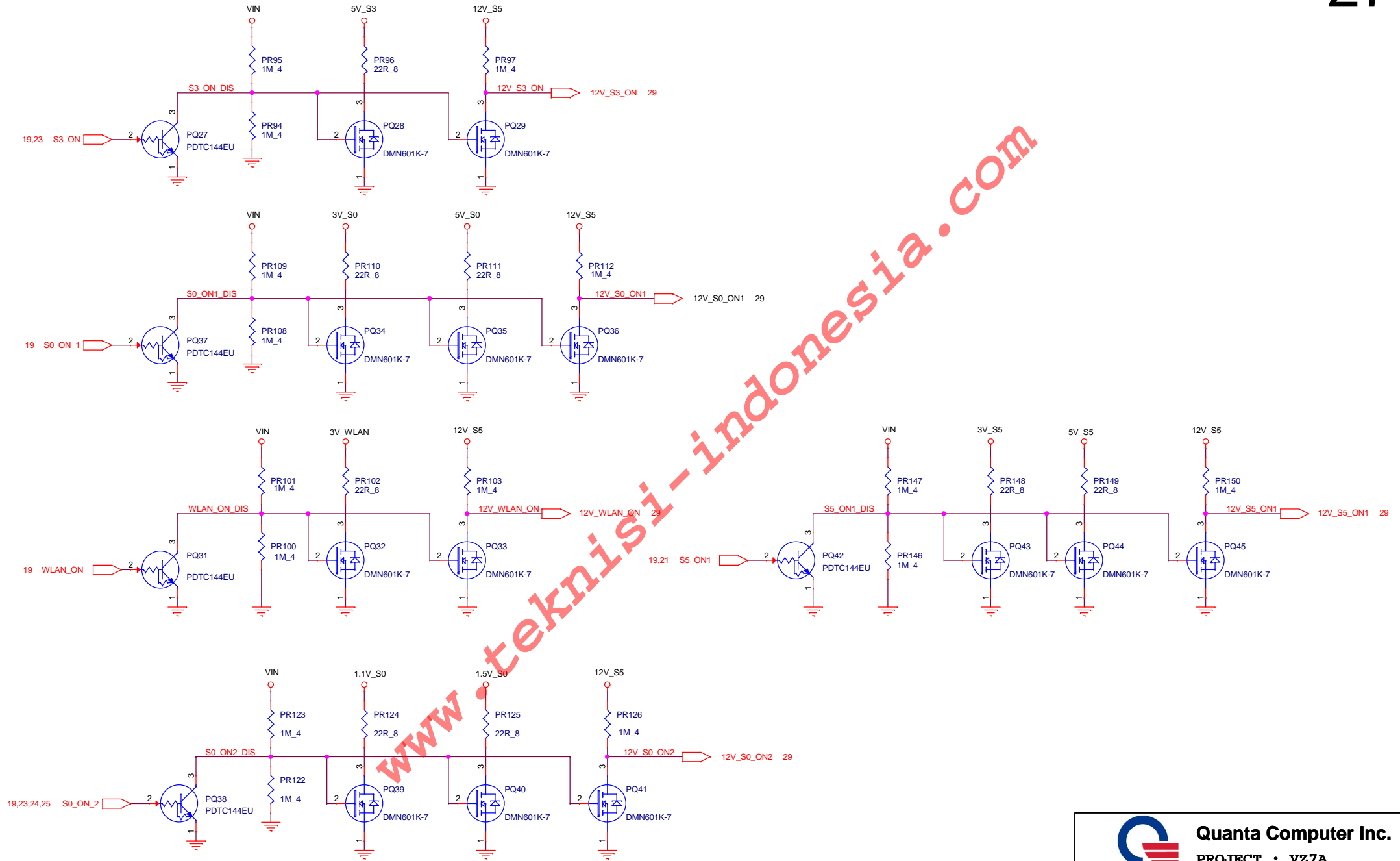


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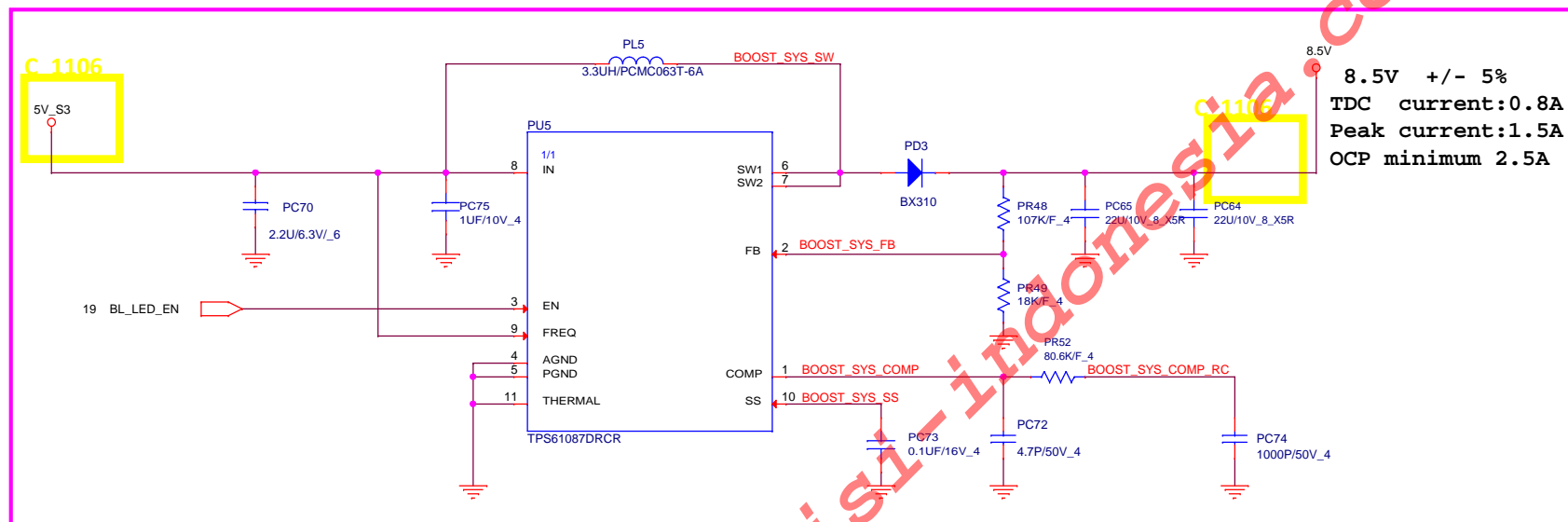
PROJECT : VZ7A

Size	Document Number	Rev
	1.1V_S5/2.5V/1.1V	1A
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Power rail discharge



B-02



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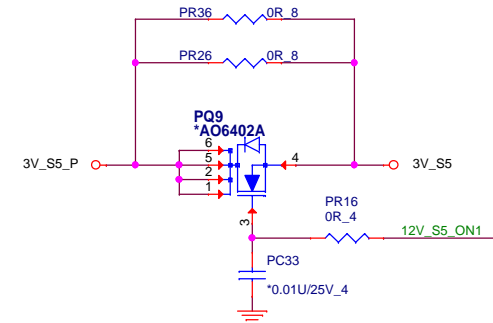
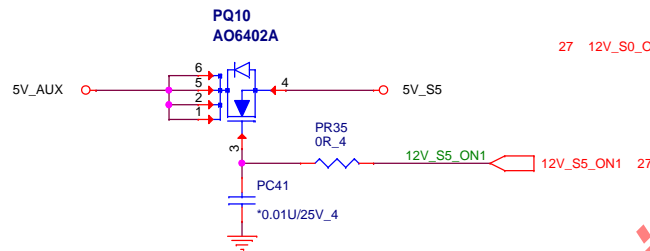
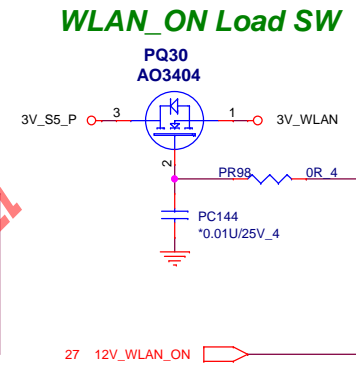
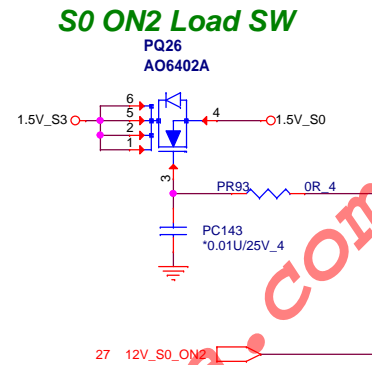
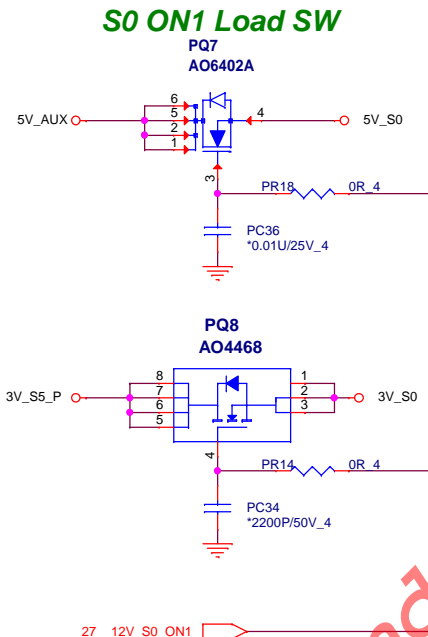
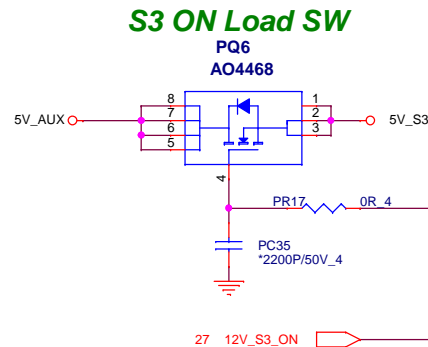
PROJECT : VZ7A

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	8.5V (TPS61087DRCR)	1A

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Load Switch

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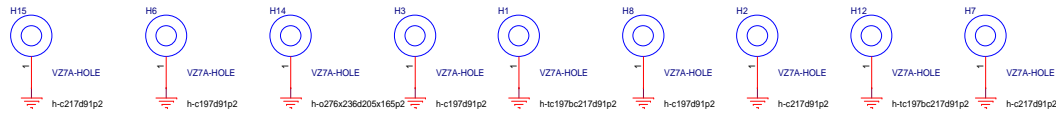


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PROJECT : VZ7A

Size	Document Number	Rev
	Load Switch	1A
Date:	Wednesday, December 26, 2012	Sheet 29 of 31

PCB fix



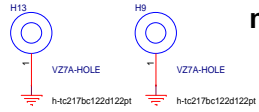
EMI for DDR

C_1108

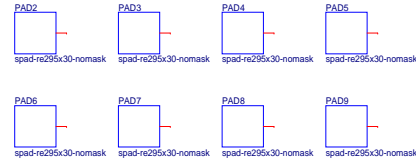
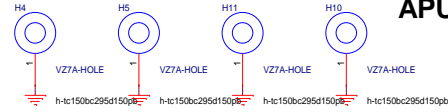


HOLE & PAD

mSATA card



APU



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